COMBINATION FIELD PROGRAMMABLE GATE ARRAY ALLOWING DYNAMIC REPROGRAMMABILITY AND NON-VOLATILE PROGRAMMABILITY BASED UPON TRANSISTOR GATE OXIDE BREAKDOWN

ABSTRACT OF THE DISCLOSURE

A cell that can be used as a dynamic memory cell for storing data or a field programmable gate array (FPGA) cell for programming is disclosed. The cell includes a capacitor having a first terminal connected to a column bitline and a second terminal connected to a switch control node. A select transistor has a gate connected to the read bitline, a source connected to the switch control node, and a drain connected to a row wordline. The switch control node stores data as a voltage indicative of a one or a zero.